BE/RTC/CBSGS/ETRX/CMOS VLSI D/N·D-17
Sem-VIII

**Q. P. Code: 11133**

**[Time: 3 Hours]** **[Total Marks: 80]**

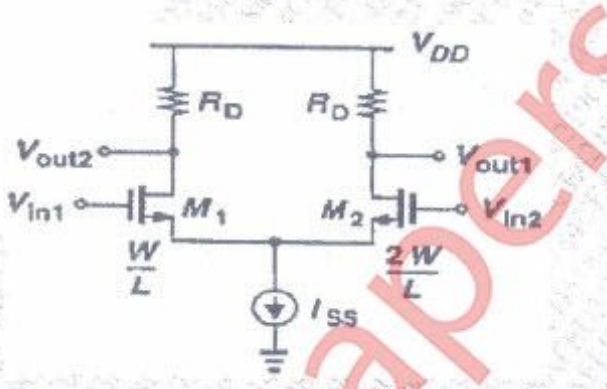
**Note: 1) Question ONE is compulsory**

**2) Solve any THREE out of remaining questions**

**3) Draw neat and clean diagrams, wherever necessary**

**4) Assume suitable data, if required**

1 (a) Analyze following circuit to get voltage gain equation if M2 is twice wide as that of M1 and Vin1=Vin2 5




(b) Explain importance of Miller Theorem 5

(c) Explain input output characteristics of phase detector (PD) circuit 5

(d) Draw and explain AMS design flow 5

2 (a) Derive expression for Voltage gain Av and output resistance Ro of Source follower stage. 10

(b) Explain in detail how to generate temperature independent references. 10

3 (a) Explain qualitative analysis of differential pair. 10

(b) Explain concept of switched capacitor circuits and hence explain switched capacitor amplifiers in detail 10

4 (a) Explain common mode response of differential pair with necessary derivations 10

(b) Explain White & Flicker noise in MOSFET. Derive equation for output and input referred noise voltage of CS stage 10

**TURN OVER**

ETRX



5 Design two stage Operational Transconductance Amplifier (OTA) to meet following specifications-. 20

$A_V > 4000$ V/V , $V_{DD}$ =2.5V, Vss=-2.5V GBW = 6MHz, $C_L$ =10pF,

SR > 10V/μs, 60° phase margin, $-2V \leq V_{out}$ range$\leq 2V$,

ICMR = -1.125V to 2V, $P_{diss} \leq 2.5$mW

Use, $K_N$=110μA/V$^2$, $K_P$= 50μA/V$^2$, $V_{TN} = |V_{TP}| = 0.7V$, $\lambda_N = 0.04V^{-1}$, $\lambda_P = 0.05V^{-1}$, Cox=2.47fF/μm$^2$. Verify that the designed circuit meets required Voltage Gain and Power Dissipation specifications.

6 (a) Give comparison between Full-custom and Semi-custom design 5

(b) Compare various opamp topologies 5

(c) Explain in detail charge pump PLL 5

(d) Write a short note on Gilbert Cell 5

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